What is claimed is:

1. A ferroelectric transistor comprising:

source and drain regions provided in a substrate; and

a gate structure on the substrate between the source and drain regions, the gate structure comprising

a conductive oxide layer overlying the substrate,

a ferroelectric material layer overlying the conductive oxide layer, and

a top electrode conductive layer overlying the ferroelectric material layer.

2. A ferroelectric transistor as in claim 1 further comprising a bottom electrode conductive layer between the conductive oxide layer and the ferroelectric material layer.

3. A ferroelectric transistor as in claim 1 wherein the electrode conductive layer is a layer of metal, a layer of conductive oxide or a multilayer of metal and conductive oxide.

4. A ferroelectric transistor as in claim 1 wherein the conductive oxide layer comprises a conductive perovskite oxide, a high temperature superconducting oxide, or an oxide film of any metal selected from a

group consisted of Mo, W, Tc, Re, Ru, Os, Rh, Ir, Pd, Pt, In, Zn, Sn, Nd, Nb, Sm, La, and V.

5. A method of fabricating a ferroelectric transistor comprising the steps of:

preparing a semiconductor substrate;

forming a gate stack on the substrate, the gate stack comprising

a conductive oxide layer overlying the substrate;

a ferroelectric material layer over the conductive oxide layer; and

a top electrode conductive layer over the ferroelectric material layer; and

forming drain and source regions on opposite sides of the gate stack.

6. A method as in claim 5 wherein the gate stack further comprises a bottom electrode conductive layer between the conductive oxide layer and the ferroelectric material layer.

7. A method as in claim 5 wherein the formation of the gate stack comprises the deposition of the multilayer gate stack, the photolithography patterning of the gate stack and the etching of the gate stack.

8. A method as in claim 5 wherein the formation of the drain and source regions comprises the implantation to a high doping concentration.

9. A method as in claim 5 further comprising the LDD ion implantation into the source and drain regions.

10. A method as in claim 5 further comprising a dielectric spacer on the sidewall of the gate stack.

11. A method as in claim 5 wherein the electrode conductive layer is a layer of metal, a layer of conductive oxide or a multilayer of metal and conductive oxide.

12. A method as in claim 5 wherein the conductive oxide layer comprises a conductive perovskite oxide, a high temperature superconducting oxide, or an oxide film of any metal selected from a group consisted of Mo, W, Tc, Re, Ru, Os, Rh, Ir, Pd, Pt, In, Zn, Sn, Nd, Nb, Sm, La, and V.

13. A method of fabricating a ferroelectric memory transistor comprising:

preparing a semiconductor substrate;

forming a replacement gate stack on the substrate, the replacement gate stack comprising

a conductive oxide layer overlying the substrate; and

a sacrificial layer over the conductive oxide layer;

forming drain and source regions on opposite sides of the replacement gate stack;

filling the areas surrounding the replacement gate stack while exposing the top portion of the replacement gate stack;

removing the sacrificial layer portion of the replacement gate stack;

forming the remainder of the gate stack, the remainder of the gate stack comprising

a ferroelectric material layer over the conductive oxide layer; and

a top electrode conductive layer over the ferroelectric material layer.

14. A method as in claim 13 wherein the replacement gate stack further comprises a bottom electrode conductive layer positioned between the conductive oxide layer and the sacrificial layer.

15. A method as in claim 13 wherein the sacrificial layer material comprises silicon nitride or silicon dioxide.

16. A method as in claim 13 wherein the filling of the areas surrounding the replacement gate stack while exposing a top portion of the replacement gate stack comprises

the deposition of a dielectric film; and

the planarization of the deposited dielectric film to expose the top portion of the replacement gate stack.

17. A method as in claim 13 wherein the formation of the remainder of the gate stack comprises

the deposition of the ferroelectric material layer;

the planarization of the ferroelectric material layer;

the deposition of the top electrode conductive layer;

the photolithography patterning of the top electrode conductive layer; and

the etching of the top electrode conductive layer.

18. A method as in claim 13 wherein the formation of the replacement gate stack comprises the deposition of the replacement gate stack, the photolithography patterning of the replacement gate stack and the etching of the replacement gate stack.

19. A method as in claim 13 wherein the electrode conductive layer is a layer of metal, a layer of conductive oxide or a multilayer of metal and conductive oxide.

20. A method as in claim 13 wherein the conductive oxide layer comprises a conductive perovskite oxide, a high temperature superconducting oxide, or an oxide film of any metal selected from a group consisted of Mo, W, Tc, Re, Ru, Os, Rh, Ir, Pd, Pt, In, Zn, Sn, Nd, Nb, Sm, La, and V.